

FLEXIBLE ANALOG-TO-DIGITAL CONVERSION AND BEAM FORMING HARDWARE

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OUTLINE

- **Division of Electronics Systems**
- **Analog-to-digital converters (ADC)**
 - High sample rate**
 - Flexible sample rate and resolution**
- **Interpolation and decimation filters**
 - Several sample rate change factors at the same time**
- **Beam forming hardware**
 - Distributed arithmetic**
 - Multiply-accumulate (MAC)**
 - Multiple constant multiplication (MCM)**
- **Conclusions**

DIVISION OF ELECTRONICS SYSTEMS

- **About 20 people in research**

3 professors, 2 associates, 2 assistants, 2 lecturers

13 PhD students, 3 engineers

- **One of four groups in STRINGENT**

Strategic Integrated Electronic Systems Research at Linköping University

System design — Technology utilization — Design efficiency

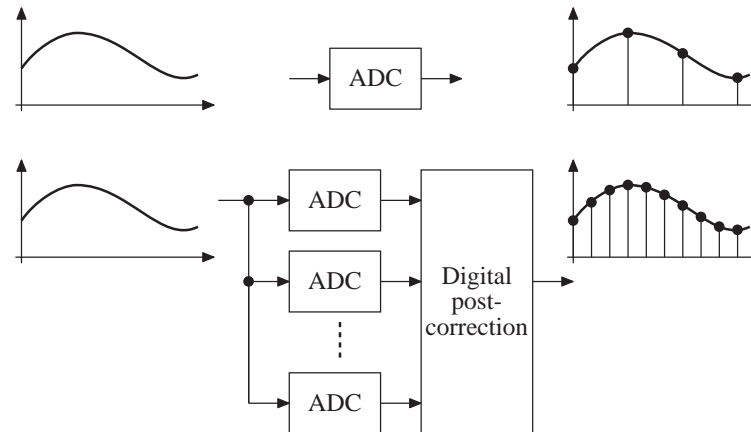
Research covers system to devices

- **Research includes the following topics**

Computational properties of digital signal processing algorithms, synthesis of application/algorithm-specific architectures, arithmetic, analog and digital filters, analog and digital circuits and systems as well as mixed analog/digital circuits

ANALOG-TO-DIGITAL CONVERTERS

- **High sample rate useful**
Less analog components (ADC closer to the antenna)
- **Parallel time-interleaved approach**



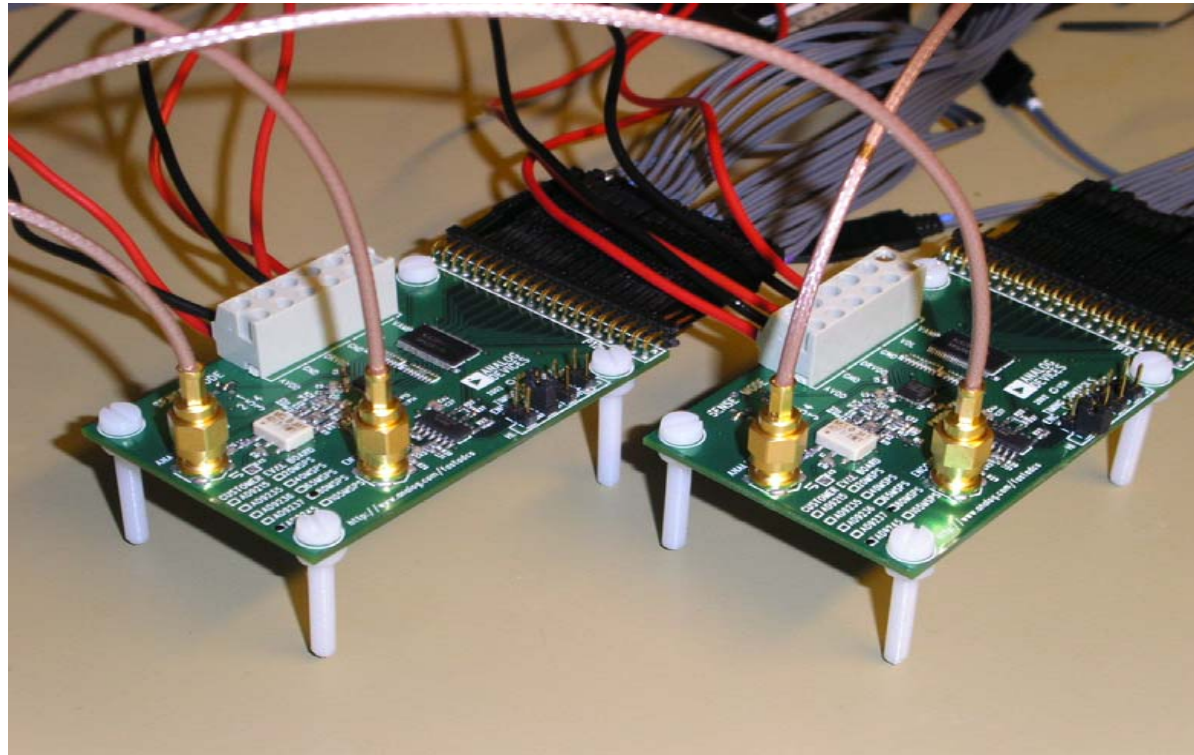
Problems with different offset, different gain, clock jitter

Digital post-processing (estimation and correction)

Spin-off company: Signal Processing Devices

ANALOG-TO-DIGITAL CONVERTERS (CONT'D)

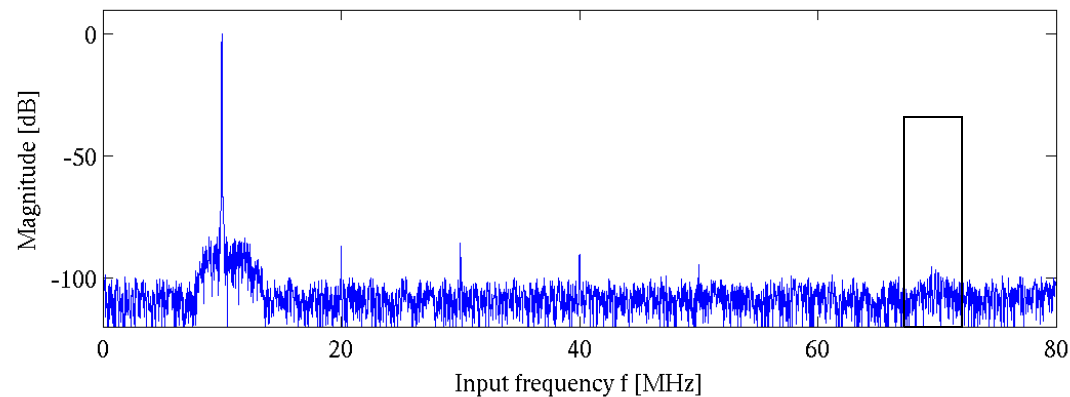
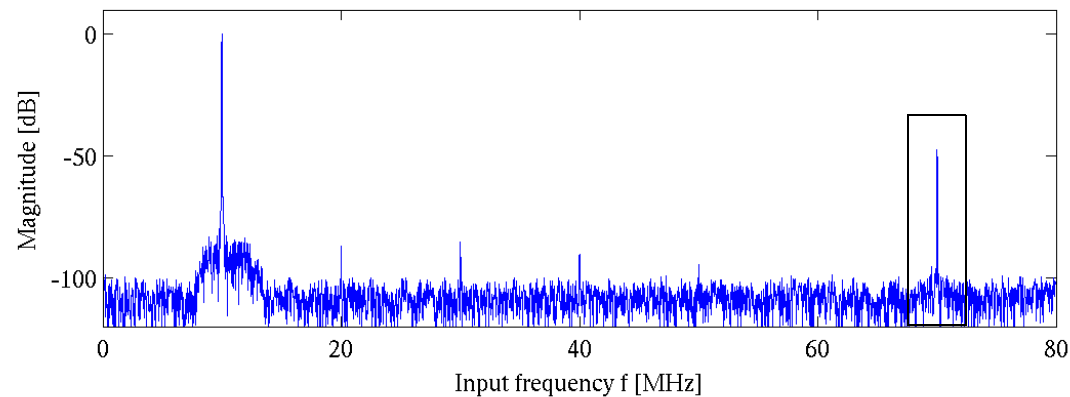
- **Experimental setup**



Standard off-the-shelf evaluation boards
Signal processing in Matlab

ANALOG-TO-DIGITAL CONVERTERS (CONT'D)

- **Experimental results (ADC running at 80 MHz)**



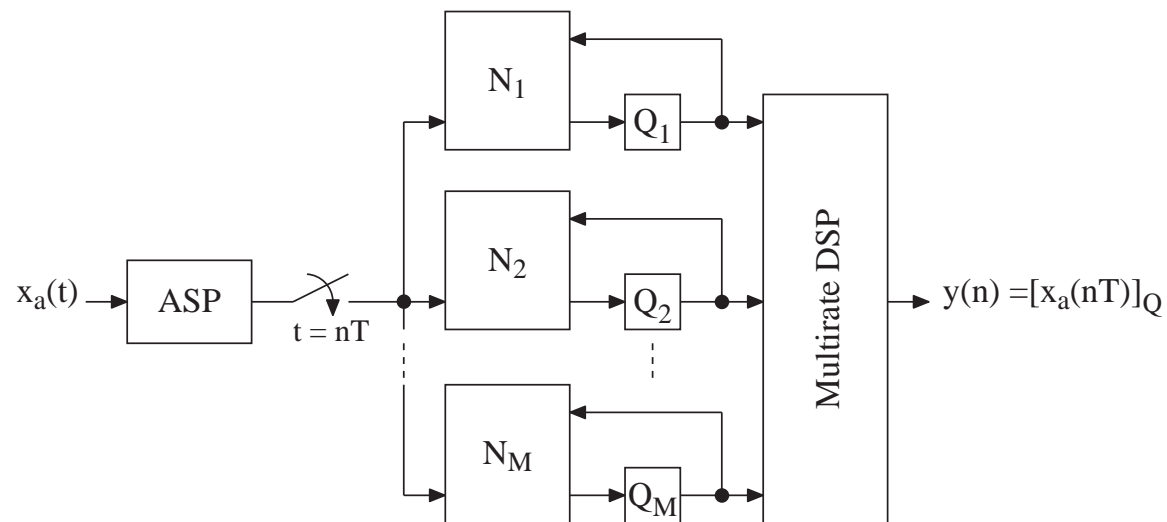
ANALOG-TO-DIGITAL CONVERTERS (CONT'D)

- **Flexible conversion**

Change the sample rate and resolution depending on the requirements

Two different approaches

- **$\Sigma\Delta$ -based approach**



Bandpass sampling — sample with lower frequency, the signal gets folded into the baseband

ANALOG-TO-DIGITAL CONVERTERS (CONT'D)

- **Change loop filter**

Change center frequency and bandwidth

- **Change sample rate**

To position the required spectrum into the baseband

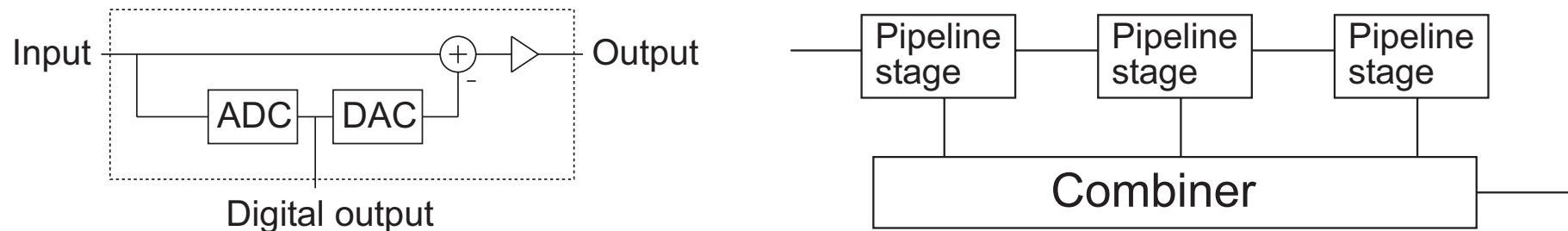
- **Parallel ADCs**

Post-processing is required for error mitigation

ANALOG-TO-DIGITAL CONVERTERS (CONT'D)

- **Pipelined ADC**

Pipelined ADC composed of several low resolution converters



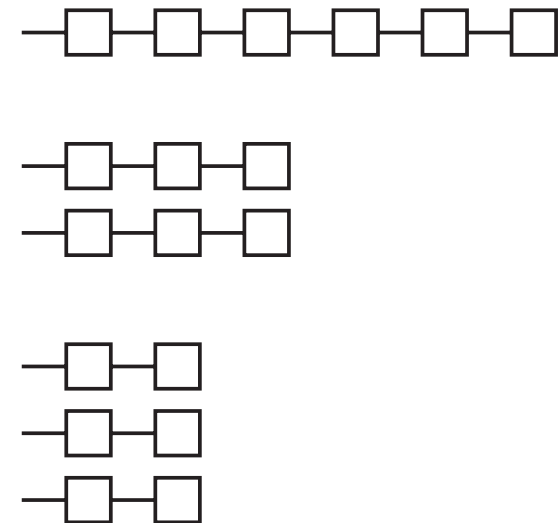
- **Flexible pipelined ADC approach**

Connect the converters differently depending on the requirements

Possible to change sample rate as well

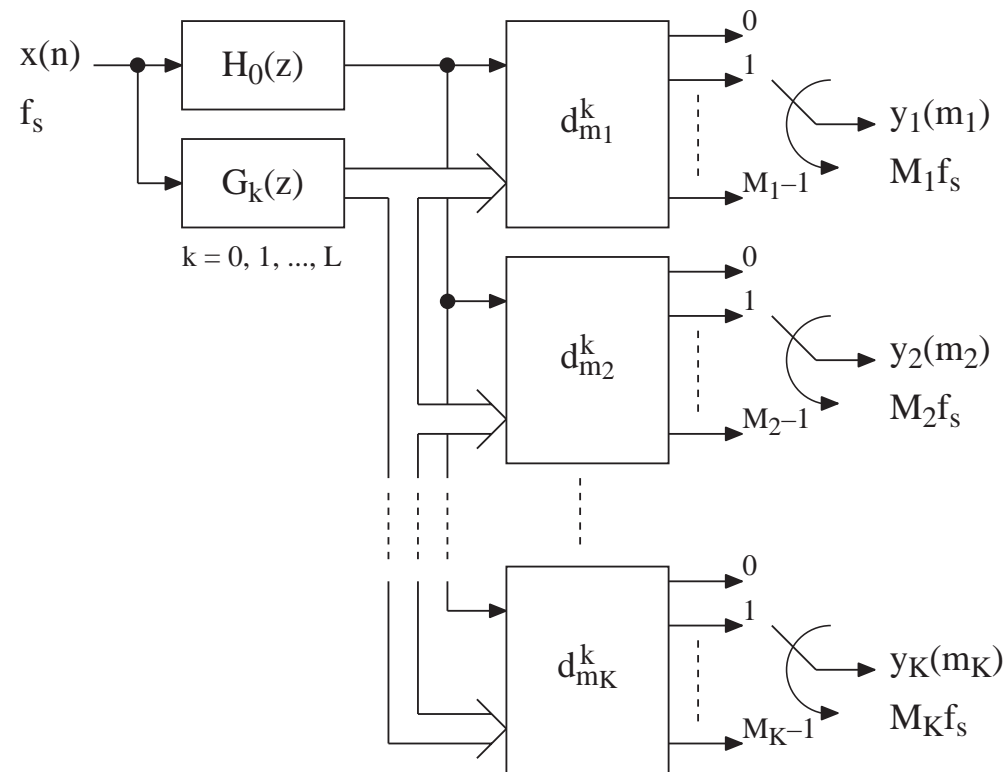
Post-processing for error mitigation required

Possible to use dynamic element matching for static errors



INTERPOLATION AND DECIMATION

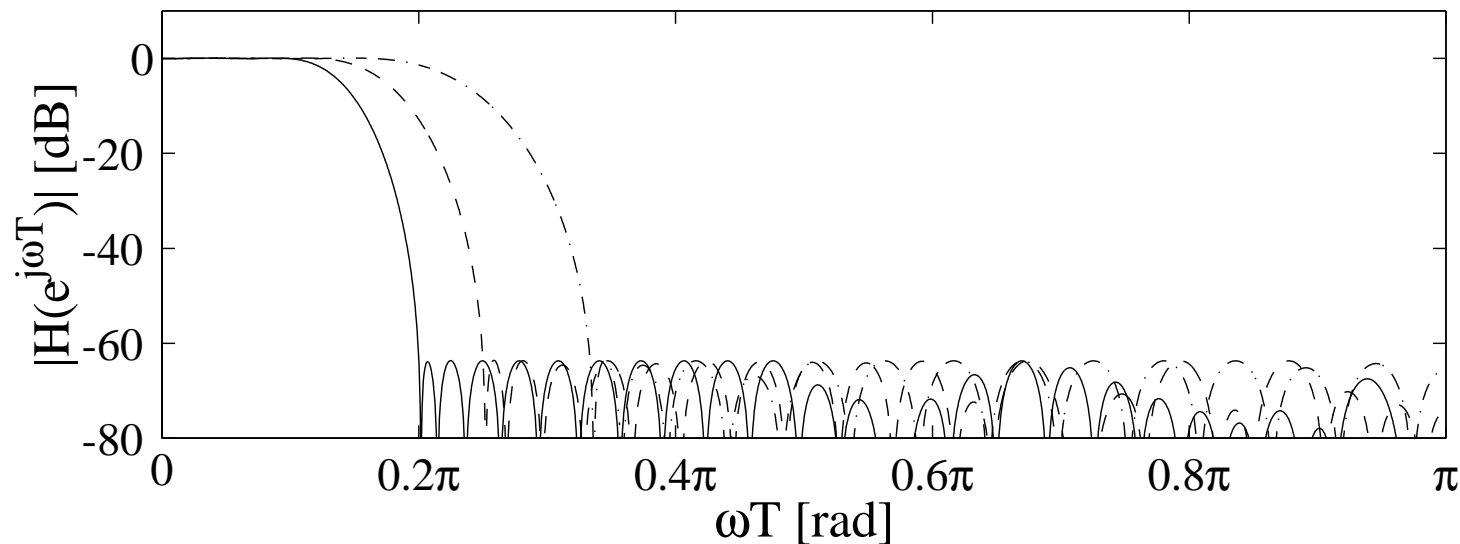
- **Filter structure with several output sample rates**



Common set of subfilters (H_0 and G_k) weighted differently
Decimation — reverse the signal flow

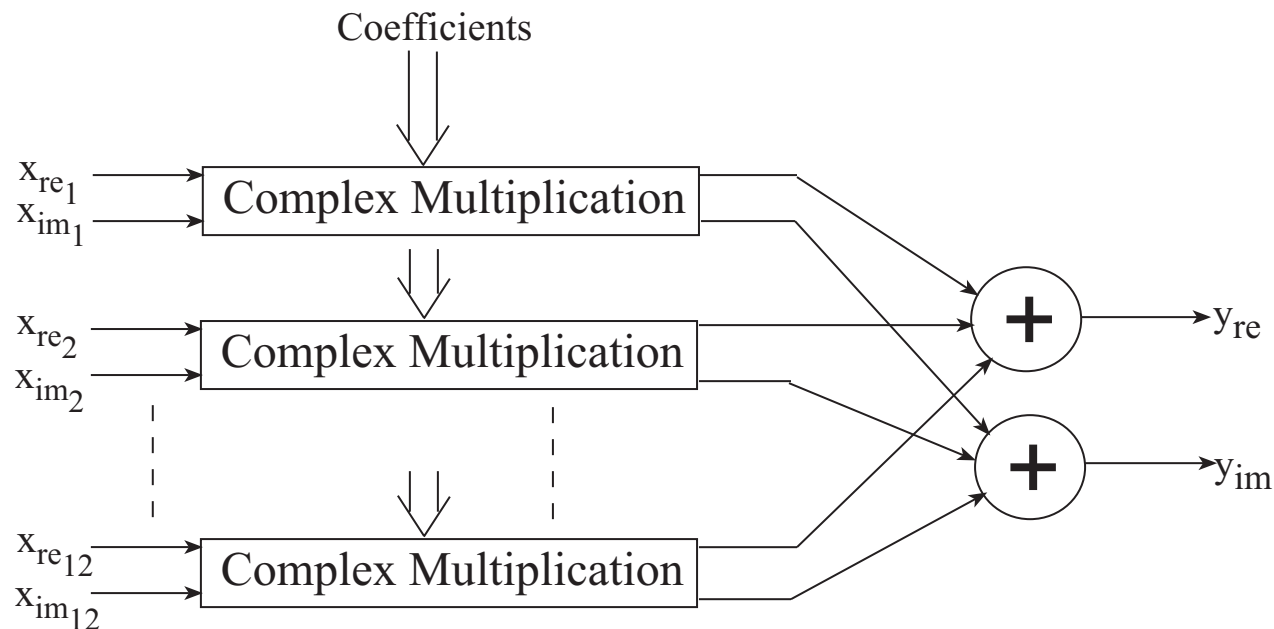
INTERPOLATION AND DECIMATION (CONT'D)

- **Low complexity compared with other approaches**
Especially when the sample rate change factors are relatively prime
- **Example filter for sample rate change of 3, 4, and 5**



BEAM FORMING HARDWARE

- **Beam forming**

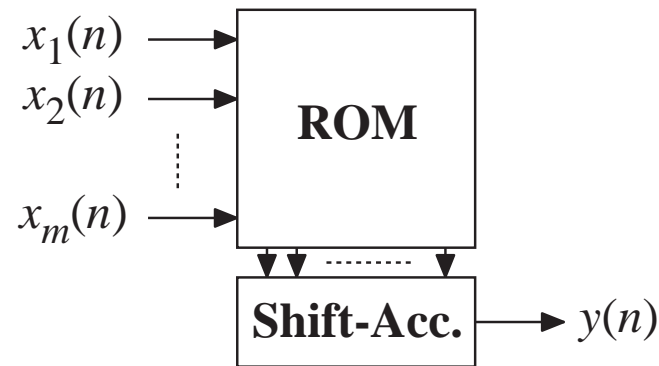


Complex numbers — previously long experience with FFT

BEAM FORMING HARDWARE (CONT'D)

- **Distributed arithmetic**

Look-up table based computation for sum of products



Each distributed arithmetic unit can compute from one complex multiplication up to a complete sum-of-products depending on the size of the look-up table

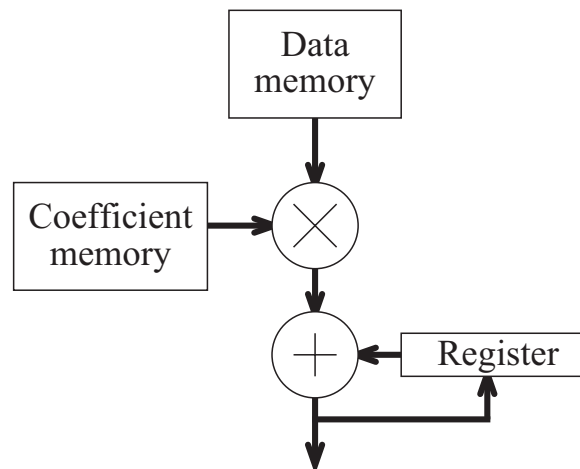
Computes one bit at a time (bit-serial processing), but can be extended to an arbitrary number of bits by exchanging the look-up tables

Previous experience with implementation in FPGA for radar applications

BEAM FORMING HARDWARE (CONT'D)

- **Multiply-accumulate (MAC) architectures**

Basic building block consisting of a multiplier and an accumulator



Commonly used in programmable DSP processors

New FPGA families have several MACs

Easy to parallelize depending on requirements

Work on computation order to minimize the power consumption

BEAM FORMING HARDWARE (CONT'D)

- **Multiple constant multiplication**

One data is multiplied with several coefficients

Transpose to get sum-of products

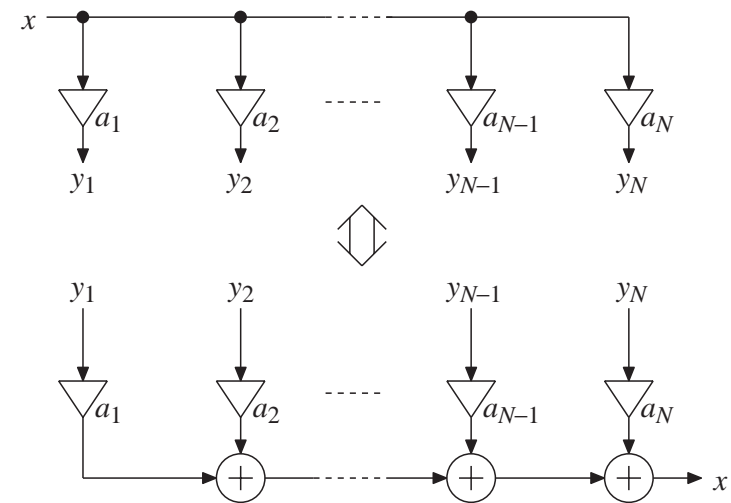
Express constant multiplier coefficients using shifts and additions/subtractions

Utilize redundancy between the coefficients to reduce the number of additions and subtractions

- **Ongoing research**

Algorithms to find efficient realizations

Power models — not only number of adders



BEAM FORMING HARDWARE (CONT'D)

- **Reprogrammability**

For distributed arithmetic and MAC-based architectures only the coefficient memories/look-up tables must be changed

For multiple constant multiplication the complete FPGA must be reprogrammed

CONCLUSIONS

- **Analog-to-digital converters**

 - High sample rates**

 - Flexible converters — trading resolution for sample rate**

- **Interpolation and decimation filters**

 - Efficient structure for several conversion factors**

- **Beam forming hardware**

 - Distributed arithmetic**

 - Multiply-accumulate (MAC)**

 - Multiple constant multiplication**